**Report 1**

# **Technical summary of experiments conducted in the lab (Steps, Results components (a screenshot with Schematic design might help), code functionality, etc...]**

## **Experiment 1: A simple inverter**

The main purpose of these experiments was to review Verilog and FPGA Refresher, as we did a simple inventor to turn on FPGA LED.

* **Steps**

After opening VIVADO, we should create design and constraint files. In the design file whose extension is **.v**. Then, we should specify the input and the output, and write the main code inside the body of the module we should assign x = ~ y. In the constraint file whose extension is **.xdc**, we should connect the input with the output ( the input bin with the output LED), by writing this code for the bin and the LED successfully.( set\_property -dict { PACKAGE\_PIN J15 IOSTANDARD LVCMOS33 } [get\_ports { SW[0] }]; #IO\_L24N\_T3\_RS0\_15 Sch=sw[0], #set\_property -dict { PACKAGE\_PIN H17 IOSTANDARD LVCMOS33 } [get\_ports { LED[0] }]; #IO\_L18P\_T2\_A24\_15 Sch=led[0]).

* **Results**

The bin labeled J15 will turn on the LED labeled H17. The LED will turn on when the bin is 0 because the FPG is actively low.

## **Experiment 2: A 4-digit 7-segment display driver**

The main purpose of these experiments was to design and implement a 4-digit 7-segment display driver module controlled by the 13 input switches.

* **Steps**

After opening VIVADO, we should create design and constraint files. In the design file, whose extension is .v, we should specify the input and output and write the main code inside the body of the module. We should write the Four\_Digit\_Seven\_Segment\_Driver module with the code given in the lap manual.

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In the constraint file, whose extension is **.xdc**, we should connect the output with the variables to set up the FPGA. The files correctly contain the written code.

* **Result**

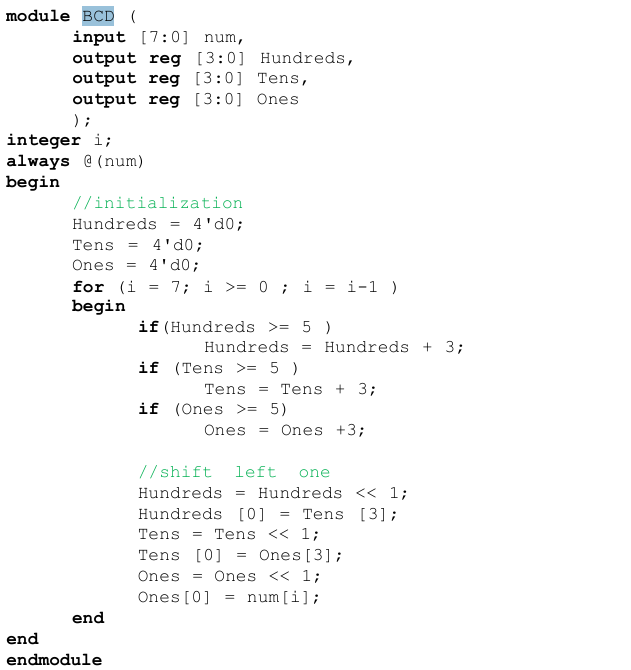
The 7-segment display driver module is controlled by the 13 input switches and will work correctly by the switches.

## **Experiment 3: A 4-digit 7-segment display driver with optimized Divisor**

This experiment is basically like the previous one (Experiment 2) with slight differences.

* **Steps**

We will use the same constraint file without any changes. However, we will use two design files Four\_Digit\_Seven\_Segment\_Driver\_Optimized.v and BCD.v. The BCD.v file contains the following code



This module helped us in the Four\_Digit\_Seven\_Segment\_Driver\_Optimized.v instead of write the code by this format

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We wrote Ones, Tens, Hundreds, and Thousands.

* Results

The result of this experiment is the same result of Experiment 2.

# **Compare the utilization and delay of experiment 2 vs experiment 3**

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| --- | --- | --- |
|  | **Experiment 1** | **Experiment 2** |
| **Utilization** | A screenshot of a computer  Description automatically generated | A screenshot of a computer  Description automatically generated |
| **Report** | The LUT Utilization of the second experiment is more than the third experiment as the second is 117 and the third is 42 (0.18% for the second experiment and 0.07% for the third one). However, the availability is the same for both experiments. The FF in Utilization and availability for both experiments is the same. IO in the second experiment (25) is more than the third experiment (24) by 1, which is 11.90% for the second experiment and 11.43% for the third one.   * **Efficiency**: The third experiment shows lower LUT utilization (0.07% vs. 0.18%), which might indicate better efficiency or less complexity in the design. * **Detail**: The second summary provides more detailed breakdowns of specific logic blocks and configurations, which could be useful for deeper analysis. * **Specifics**: The third experiment provides more details on IO and memory, which could be crucial depending on the design requirements. | |
| **Timing summary**  **hold** | A screenshot of a computer  Description automatically generated | A screenshot of a computer  Description automatically generated |
| **Report** | There is a significant difference between both experiments in the total, logic, and net delays, as it shown that the the delay of third experiment is less that the delay of the second one. | |
| **Timing summary**  **Setup** | A screenshot of a computer  Description automatically generated | A screenshot of a computer  Description automatically generated |
| **Report** | There is a significant difference between both experiments in the total, logic, and net delays, as it shown that the the delay of third experiment is less that the delay of the second one.  This means that in terms of timing and delay, the third experiment is more efficient than the second experiment. | |